



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,433	09/01/2006	Mikio Izumi	295880US2PCT	1754
22850	7590	01/04/2010	EXAMINER	
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314				CRAIG, DWIN M
ART UNIT		PAPER NUMBER		
		2123		
NOTIFICATION DATE			DELIVERY MODE	
01/04/2010			ELECTRONIC	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com  
oblonpat@oblon.com  
jgardner@oblon.com

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/591,433	IZUMI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	DWIN M. CRAIG	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 21 October 2009.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-9, 11-15 is/are rejected.
- 7) Claim(s) 10 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ .  | 6) <input type="checkbox"/> Other: _____ .                        |

## **DETAILED ACTION**

1. Claims 1-15 have been presented for reconsideration based on Applicants' responses, arguments and amended claim language.

### ***Response to Arguments***

2. Applicants' arguments presented in the October 21<sup>st</sup> 2009 responses have been fully considered; the Examiner's response is as follows:

2.1 The Examiner thanks the Applicants' for providing an amended specification in idiomatic English and hereby withdraws the previous objection to the same. The substitute specification has been entered.

2.2 The Examiner thanks the Applicants' for amending the claim language and hereby withdraws the earlier applied 35 U.S.C. 112 2<sup>nd</sup> paragraph rejections of claims 1-15. However, the Examiner notes that the following amended limitation, "input logic patterns have been verified in advance of installation of the logic circuitry in the safety protection system", merely teaches an intended use of the logic system and therefore has very little patentable weight. Any teaching of logic that is being verified in an emulation or simulation or test meets the scope of the claimed *verification* in that these logic systems will eventually be implemented into a hardware device after they have been simulated, emulated or tested.

2.3 The Examiner has found Applicants' arguments as regards the previously applied obviousness type double patenting rejections to be persuasive. The change of scope of the current claim language is no longer an obvious variation of the claimed subject matter as set forth in U.S. Patent 7,512,917.

**2.4** As regards Applicants' response to the 35 U.S.C. 102 and 35 U.S.C. 103(a) rejection of claims 1-15, in view of the newly amended claim language the Examiner hereby withdraws the previously applied prior art rejections of claims 1-15. More specifically the newly amended claimed limitation: "a functional module formed by combining the plurality of functional units so as to form a logic structure in which the logic structure of the combination of the plurality of functional units is different from the logic structure of each of the plurality of functional units individually" is not currently disclosed in the prior art of record.

**2.5** A new search based on the newly amended claim limitations has revealed new art.

#### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**3.** Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**3.1** Claim 3 discloses the following, *a functional unit whose performance has been verified in advance*, and yet it is unclear from the claim language exactly in advance of what event the logic is being verified. Further, independent claim 1 has been amended to state that the logic patterns of the functional units have been verified in advance of installation of the logic circuitry in the safety protection system and it is unclear if the claimed verification in claim 3 is taking place before the claimed installation or after another, as yet undisclosed event.

Clarification and/or amendment is requested.

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3, 7, 9, 11, 13, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over by “Applying Build-In Self-Test to Majority Voting Fault Tolerant Circuits” hereafter referred to as *Stroud et al.* in view of U.S. Patent 5,036,473 to Butts et al.

**4.1** As regards independent claims 1 and 13 and using claim 1 as an example, *Stroud et al.* discloses, *a safety protection instrumentation system for a nuclear reactor constructed using digital logic* see page(s) 305 & 306 in the section entitled “Verification and Simulation Results”.

wherein digital logic includes functional units (see Figure 2 "Circuit Module 1" Circuit Module 2" etc...) in which output logic patterns correspond to all input logic patterns are verified in advance and a functional module formed by combining the functional units (as regards verification see page(s) 305 & 306 as regards a teaching of output logic patterns and input logic patterns see the discussion regarding test pattern generators in the portion of *Stroud et al.* entitled “3. BIST for Fault Tolerant Circuits” as regards the teaching so input logic patterns see the sentence in section 3. BIST for Fault Tolerant Circuits “As a result, detecting the presence of single and multiple faults will indicate a need for potential system repairs in the future but, the majority voting fault tolerant circuit must then be tested for its ability to mask these faults and provide the *correct output response for any given input stimuli.*” *Emphasis added*). As regards the newly amended limitation, input logic patterns have been verified in advance of installation of the logic circuitry in the safety protection system, *Stroud et al.* teaches the use of a BIST or Built-In-Self-Test, which performs a test, therefore the claimed verification is being performed before the logic is actually being installed which meets the call of the current claim language.

However, *Stroud et al.* does not expressly disclose, a functional module formed by combining the plurality of functional units so as to form a logic structure in which the logic structure of the combination of the plurality of functional units is different from the logic structure of each of the plurality of functional units individually.

*Butts et al.* teaches, a functional module formed by combining the plurality of functional units so as to form a logic structure in which the logic structure of the combination of the plurality of functional units is different from the logic structure of each of the plurality of functional units individually (See Figures 14, 15 and 16, note that the resultant output from the combined plurality of identical logic units will be different from the output of just one of the logic units, for one example the output of functional units in Figure 15 such that the logic structure of the combination of logic units will be different than just the output of one of the logical units, for example there will be three logical inputs instead of just one, see also Figure 45b & 48c and Col. 12 lines 15-28 and Col. 33 lines 17-31 which describes Fault Simulation, Fault Simulation test a system to see if the current logic configuration is functioning correctly, further Col. 18 lines 60-68 and Col. 19 lines 1-62 as well as Col. 20 lines 1-5 teaches the specifics of how the logic modules are connected to form a new logic configuration whose output is different from the output of the different logic modules individually).

*Stroud et al.* and *Butts et al.* are analogous art because they both come from the same problem solving area of logic system verification and testing.

At the time of the invention, it would have been obvious, to a person of ordinary skill in the logic arts, to have used the teachings of *Butts et al.* in combination with the teachings of *Stroud et al.* in order to obtain the invention as specified in claims 1-3, 7, 9, 11, 13, 14 and 15.

The motivation for doing so would have been, to provide a method and a system to test and configure blocks of logic in order to determine if the final system is fail-safe for use in a mission critical environment such as a safety protection system.

Further and in regards to the requirement for a teaching, suggestion and/or motivation please see *Dann v. Johnson*, 425 U.S. 219, 189 USPQ 257 (1976) and *Leapfrog Enterprises, Inc. v. Fisher-Price, Inc.*, --F.3d--, 82 USPQ2d 1687 (Fed. Cir. 2007) as well as *KSR International Co. v. Teleflex Inc.*, 550 U.S. --, 82 USPQ2d 1385 (2007). The cited cases recently decided by the Federal Circuit Court as well as the U.S. Supreme Court clearly set forth that the references themselves do not have to expressly disclose a teaching, suggestion or motivation to combine references in an obviousness type of art rejection.

Therefore, it would have been obvious to combine the teachings of *Butts et al.* with the teachings of *Stroud et al.* in order to obtain the invention as specified in claims 1-3, 7, 9, 11, 13, 14 and 15.

**4.2** As regards claim 2, *Stroud et al.* discloses, wherein, each of the functional units individually implements the output logic patterns resulting from the input logic patterns solely on hardware, and determines whether the output values coincide with predicted values calculated from design specifications, (see Figure 1 and the discussion regarding test patterns).

**4.3** As regards claim 3, *Stroud et al.* discloses, duplicate circuit modules, see the discussion on the page with Figure 2 repeated here... “Given the same initialization values, each *replicated circuit* would ideally be tested with identical sets of test patterns, compacting identical output responses.” Replicated circuits will have same gate structure.

**4.4** As regards claim 7, *Sroud et al.* discloses, wherein the safety protection instrumentation system is structured so as to generate input patterns in accordance with design specifications of the functional module and to determine whether the output patterns corresponding to the input patterns in the functional module coincide with predicted values calculated from the design specifications. (see the section entitled, "3. BIST for fault tolerant circuits" a portion of which is repeated here; *These two testing requirements (the ability to detect all multiple stuck-at faults and the ability to verify proper operation in the presence of compensating module faults) have several implications on BIST when applied to fault tolerant circuits as well as on the structure of the fault tolerant circuit. In order to facilitate verification of proper operation in the presence of faults, test pattern generators (TPGs) must be placed at the inputs of the replicated circuit modules while output response analyzers (ORAs) must be placed at the outputs of the MVCs. The TPG placement provides for single and multiple stuck-at fault detection in the replicated circuit modules as well as the MVCs [4] while the ORA placement allows the MVCs to mask compensating module faults. When implementing the fault tolerant circuit, the MVCs should be placed between the outputs of the replicated combinational logic functions and the inputs to the replicated flip-flops. This MVC placement allows the TPG and ORA circuits to be constructed from the flip-flops of the fault tolerant circuit. The output response analyzers will determine whether the output patterns corresponding to the input patterns in the functional module coincide with predicted values calculated from the design specifications.*

**4.5** As regards claim 9, *Sroud et al.* discloses, wherein the safety protection instrumentation system performs addition or comparison of two variables in the functional unit to replace either

one of the two variables with a constant that can be specified with an address having the number of bits smaller than that of the variable, (replacing a variable with a constant is being interpreted to be performing a stuck bit test, see the abstract).

**4.6** As regards claim 11, *Stroud et al.* discloses, wherein the functional unit has a function of calculating maximum and minimum output values by a simple expression and a function of passing the maximum and minimum output values, and wherein the safety protection instrumentation system includes a trip evaluator that compares signal values with the maximum and minimum output values to determine whether the signal values are appropriate and an abnormality diagnosis circuit that outputs an abnormal operation signal, See the section entitled, “3. BIST for Fault Tolerant Circuits”.

**4.7** As regards claim 14, *Stroud et al.* discloses, wherein data processing in the functional units in the safety protection instrumentation system is serially performed in the order of connection, and the serial transmission of a signal is confirmed by monitoring an output timing and it is determined whether the signal is output as designed to verify the performance of the safety protection instrumentation system, see section 1.2 Modified Circular BIST a portion of which is presented here, “The structure is designed to operate either in one Circular BIST chain that incorporates the whole circuit or in R separate, but identical, Circular BIST chains that partition each set of circuit modules and MVCs. Multiplexers sharing a common control input are incorporated between each of the R input and output sections of the Circular BIST chain to configure the chain into the one large chain or R identical chains.”, Verifying the structure in R

separate, but identical BIST chains is functionally the same as performing the verification in a serial manner.

**4.8** As regards claim 15 *Stroud et al.* teaches, comprising the step of verifying whether the functional units in the safety protection instrumentation system have same structure as an internal structure when performance of the functional units is verified, See the section entitled, “3. BIST for fault tolerant circuits”.

**5.** Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of *Butts et al.* as applied to claims 1 and 13 above and in further view of U.S. Patent 6,587,979 to *Kraus et al.*

The teachings of *Stroud et al.* as modified by the teachings of *Butts et al.* disclose the verification of a reactor safety system by combining logic elements of an identical structure to form a new logic structure that is different from the original logic structure as expressly claimed in independent claims 1 and 13, see above, in that their combined teaching lacks;

**5.1** As regards claim 4, neither *Stroud et al.* nor *Butts et al.* expressly disclose, wherein the functional module formed by combination of the functional units includes a register thorough which an output from the functional unit is transmitted and a delay element used for adjusting the timing of signal processing in the functional unit.

However, *Kraus et al.* teaches a programmable delay to assist in circuit testing, see “A skew circuit 81 adjustably delays each of the DI, ADDR and CNT outputs of data generator 60, filters 78 and 80, and sequencer 72 with delays controlled by the SKEW data input from JTAG

register 55 of FIG. 6. The delays are set to accommodate the timing requirements of the RAM under test.”, in Col. 16 lines 29-34.

*Stroud et al.*, *Butts et al.* and *Kraus et al.* are analogous art because they both come from the same problem solving area of circuit testing and verification.

At the time of the invention, it would have been obvious to an artisan of ordinary skill to have used the delay methods of *Kraus et al.* to verify the safety protection circuits of *Stroud et al.* and *Butts et al.*.

The motivation for doing so would have been, to provide a build-in test circuit in an embedded system to test circuits without having to provide a custom BIST after the design has been complete and to therefore make verification of circuits easier, see Col. 2 lines 32-56 of *Kraus et al.*

Therefore, it would have been obvious to combine the teachings of *Kraus et al.* with the teachings of *Stroud et al.* and *Butts et al.* in order to obtain the invention as specified in the claim 4.

**6.** Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of *Butts et al.* as applied to claims 1 and 13 above and in further view of U.S. Patent 5,805,608 to Baeg et al.

The teachings of *Stroud et al.* as modified by the teachings of *Butts et al.* disclose the verification of a reactor safety system by combining logic elements of an identical structure to form a new logic structure that is different from the original logic structure as expressly claimed in independent claims 1 and 13, see above, in that their combined teaching lacks;

*Stroud et al.* as modified by *Butts et al.* does not expressly disclose, wherein the functional module formed by a combination of the plurality of functional units further comprises a register through which an output from at least one functional unit is transmitted wherein the system uses handshaking for transferring a signal from the functional unit that drives the register at different clock frequencies, among the functional units.

However, *Baeg et al.* teaches a programmable clock used for BIST testing in logic circuits see Figure(s) 2F and 4 and Col. 2 lines 64-67 and Col. 3 lines 1-67 and Col. 4 lines 1-3 more specifically “in some manufacturing tests, clocks pscA, pscB are non-overlapping clocks having equal frequencies”, which clearly infers that in other configurations there are clocks of different frequencies, see also Table 1, as regards a teaching of handshaking see the descriptive text.

*Stroud et al.*, *Butts et al.* and *Baeg et al.* are analogous art because they both come from the same problem solving area of circuit testing and verification.

It would have been obvious, at the time of the invention, to an artisan of ordinary skill to have used the clock frequency teachings of *Baeg et al.* with the safety circuit verification teachings of *Stroud et al.* and logic circuit teachings of *Butts et al.*.

The motivation for doing so would have been because it is desirable to provide simple clock generation circuitry, see *Baeg et al.* Col. 1 lines 15-42.

Therefore it would have been obvious to combine the teachings of *Baeg et al.* with the teachings of *Stroud et al.* and *Butts et al.* in order to obtain the invention as specified in the claim 5.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of *Butts et al.* as applied to claims 1 and 13 above and in further view of U.S. Patent 6,691,079 to Lai et al.

The teachings of *Stroud et al.* as modified by the teachings of *Butts et al.* disclose the verification of a reactor safety system by combining logic elements of an identical structure to form a new logic structure that is different from the original logic structure as expressly claimed in independent claims 1 and 13, see above, in that their combined teaching lacks;

*Stroud et al.* as modified by *Butts et al.* does not expressly disclose, *wherein the safety protection instrumentation system further comprises; software which describes effective programs statements executed by hardware and input pattern groups indicating operation paths, uses branch coverage or toggle coverage for evaluating the ratio of the input logic patterns or determining whether the number of the input patterns is sufficient, and determines whether the output logic patterns corresponding to the input logic patterns coincide with predicted patterns calculated from design specifications to verify the connection between the functional units.*

However, *Lai et al.* teaches, branch coverage and toggle coverage, see Col. 5 lines 59-67 and Col. 6 lines 1-15.

*Stroud et al.*, *Butts et al.* and *Lai et al.* are analogous art because they both come from the same problem solving area of digital circuit verification.

At the time of the invention, it would have been obvious to a person of ordinary skill in the logic verification art to have used branch coverage and toggle coverage when performing verification of a logic circuit.

The motivation for doing so would have been to provide a method of performing test coverage on a logic circuit design in less time and therefore perform the tests with greater efficiency, see Col. 1 lines 50-54 of *Lai et al.*

Therefore it would have been obvious to use the test coverage teachings of *Lai et al.* with the logic circuit verification teachings of *Stroud et al.* and the logic module teachings of *Butts et al.* in order to obtain the invention as specified in claim 6.

**8.** Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of *Butts et al.* as applied to claims 1 and 13 above and in further view of U.S. Patent 5,621,776 to Gaubatz.

The teachings of *Stroud et al.* as modified by the teachings of *Butts et al.* disclose the verification of a reactor safety system by combining logic elements of an identical structure to form a new logic structure that is different from the original logic structure as expressly claimed in independent claims 1 and 13, see above, in that their combined teaching lacks;

**8.1** As regards claim 8, *Stroud et al.* and *Butts et al.* does not expressly disclose, *wherein the safety protection instrumentation system includes an analog-to-digital element that converts an analog signal pattern in accordance with design specifications of the functional module into a digital value to generate a digital input pattern and a digital-to-analog element that converts an output corresponding to an input in the functional module into an analog value, and determines whether the analog value coincides with a predicted value calculated from the design specifications.*

However, *Gaubatz* teaches analog signals being used in Fault-Tolerant Reactor Protection Systems, see Figure 3 as well as Col. 8 lines 54-67 and Col. 9 lines 1-40.

*Stroud et al.*, *Butts et al.* and *Gaubatz* are analogous art because they both come from the same problem solving area of Nuclear reactor protection systems.

At the time of the invention, it would have been obvious to a person of ordinary skill to have provided for analog signals in a reactor fault tolerant protection logic circuit.

The suggestion for doing so is provided in *Gaubatz* in Col. 2 lines 25-33 which provides the requirements for a reliable reactor protection system and using analog signals in a test of a fault tolerant logic system for use in nuclear reactors would be required in order to test the entire system.

Therefore, it would have been obvious to use the teachings of *Gaubatz* with the teachings of *Stroud et al.* and *Butts et al.* in order to obtain the invention as specified in claims 8 and 12.

**8.2** As regards claim 12, *Stroud et al.* and *Butts et al.* do not expressly disclose, *wherein the safety protection instrumentation system further comprises a first safety protection instrumentation system that converts a digital output into an analog value and converts the analog value into an optical signal and a second safety protection instrumentation system that converts the optical signal into an analog value and converts the analog value into a digital value, and wherein the first safety protection instrumentation system is connected to the second safety protection instrumentation system.*

However, *Gaubatz* teaches, an analog to digital converter, see Col. 7 lines 7-10 and an optical signal, see Col. 7 lines 44-65.

***Allowable Subject Matter***

9. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

While *Stroud et al.* teaches verification of a reactor safety system and *Butts et al.* teaches logic modules and Dennis et al. teaches flags in a reactor protection system, **none of the prior art of record teaches or discloses**, (claim 10), “wherein the functional unit has a function of passing an operation flag indicating normal completion of the operation, wherein the functional module has a function of monitoring the operation flag, and wherein the safety protection instrumentation system further comprises: a trip evaluator that receives an output from the functional module and determines whether the operation flag is set; and an abnormality diagnosis circuit that outputs an abnormal operation signal if the operation flag is not set.”, in combination with **all** of the features and elements comprising the currently amended claim 1.

**Comments**

9.1 After careful re-consideration and a review of the prior art the Examiner has determined that the exact limitations as expressly disclosed in dependent claim 10 are not disclosed or suggested by the prior art of record.

***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DWIN M. CRAIG whose telephone number is (571)272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

Art Unit: 2123

applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dwin M Craig/  
Examiner, Art Unit 2123